New Horizon College of Engineering

Department of Electronics and Communication Engineering

BOARD OF STUDIES MEETING - 3

DATE: 04/07/2017

VENUE: Boardroom, MBA Department

Time: 10 AM to 1:30 PM

New Horizon College of Engineering

Department of Electronics and Communication Engineering

BOARD OF STUDIES MEETING - 3

DATE: 04/07/2017

VENUE: Boardroom, MBA Department

Time: 10 AM to 1:30 PM

AGENDA

1. Discussion on Scheme and Syllabus of B.E Courses from 2nd to 4th year.
2. Approval of B.E. syllabus for 3rd year.

Members of Board of Studies

MEMBERS OF THE BOARD OF STUDIES

Sl.No.		Name
1.	Faculty with different specialization	Mr. Aravinda K, Sr. Asst. Professor, ECE, NHCE
2.		Ms. Dharmambai, Sr. Asst. Professor, ECE,NHCE
3.		Dr. Mohan Kumar Naik, Sr. Associate Professor, ECE, NHCE
4.		Dr. Nisha KCR, Associate Professor, ECE, NHCE
5.		Ms. Ishani Mishra, Sr. Assistant Professor, ECE,NHCE
6.	Subject Expert	Dr. Seshachalam, HOD,BMS
7.		Dr. B K Sujatha, Professor,MSRIT
8.	VTU Nominee (Expert-VC)	Dr. Preeta Sharan, Professor, Oxford College of Engineering
9.	Industry	Mr. Ravishankar, Director, Anora laboratories Pvt Ltd.
10.		Mr. Nagaraj Subramaniam, Eklakshya, Ex GM, TI
11.		Dr. Prasad, MD, Audience Communication
12.	Co-opted member	Ms. Lipsa Dash, Assistant Professor, ECE,NHCE
13.		Ms. Divya Sharma, Sr. Assistant Professor, ECE,NHCE
14.	Student-PG Alumni	Mr. Praveen Kumar J, M.Tech, e silicon Tech

MINUTES OF THE 3RD MEETING OF THE BOARD OF STUDIES FOR AY 2017-18

1. Welcome and Introductory remarks by the BOS Chairman

The Chairman welcomed VTU Nominee, expert members from academics and industry and other members of the Board of Studies and highlighted the following salient points for discussion in the 3rd BOS Meeting.

- Curriculum (Scheme) design for B.E. program from 2nd to 4th year.
- Introduction of the syllabus for Third Year B.E. program in Electronics & Communication Engineering.

Introductory remarks by the BOS Chairman

1. Chairman remarked on the need of accreditation process which is predominantly outcome based aiming at giving more weightage to the curriculum design, execution and outcome.
2. Chairman also mentioned about the 3 levels of expectation by the NBA namely the achievement of course outcomes, program outcomes and the program educational objectives.
3. Chairman mentioned that different guidelines such as that proposed by AICTE, Lead Professional Societies and VTU are available on the curriculum structure i.e., number of courses to be offered under for B.E. program.
4. Chairman sought opinion of industry experts on curriculum design and structure that could promote learning and impart industry-specific skills most importantly technical. He also invited responses from the external academic experts on the same.

Remarks by Experts and Members

1. Industry expert informed that industry is keen for engineers who have practical exposure and ability to apply what is learnt in the courses and suggested that these attributes could be developed in the student by working collaboratively with the industry through industry projects or industry sponsored research.

2. Academic expert suggested regrouping of courses so as to offer selection to students from different bundles such as VLSI, Communication and Signal Processing, IOT and Embedded, Networking etc. implementing flip the class method for targeted limited courses and identifying selected subjects with industry components.
3. One expert member opined inclusion of self-study in core courses where students are given scope for paper survey, projects etc.

2. The Board of Studies in Electronics & Communication Engineering recommended the following

The Standing Committee recommended

- that the revision of syllabus of the following course namely

16ECE34 LOGIC DESIGN

renamed as "**Digital Electronics Circuits"** with syllabus as in **Appendix I** be ratified and that this takes effect for the batches of students in AY 2017-18.

- that the merging of the following core courses namely

16ECE34 Electronic Circuits-I

16ECE43 Electronic Circuits-II

into one course Renamed as "**Analog Electronics Circuits"** with syllabus as in **Appendix I** be approved and that this takes effect for the batches of students in AY 2017-18.

- that the following course namely

16ECE33 Programming with Data structures

to be moved from 3rd semester to 5th Semester and be categorized as Professional Elective course.

- that the revision of the following course namely

16ECE36 Signals and Systems

to be approved by removing the practical component of the course.

- that the replacement of the following course in 4th Semester named

16ECE43 Electronic Circuits-II

with **"Linear Integrated Circuits"** syllabus as in **Appendix I** be ratified and that this takes effect for the batches of students in AY 2017-18.

- that the credits pertaining to removal of practical component of the following course

16ECE36 Signals and Systems and

the merging of the following core courses namely

16ECE34 Electronic Circuits-I

16ECE43 Electronic Circuits-II

be compensated by including "**Mini Project-I**" in 3rd Semester and "**Mini Project-II**" in 4th Semester as in **Appendix I** be approved.

The B.E. scheme of batch 2015-19 and batch 2016 – 2020 is included in **Appendix II.**

3. Vote of Thanks by the Chairman- BOS

The meeting concluded with the vote of thanks by the chairman (HOD, ECE Department). He appreciated the comments from all the experts, faculty and student alumni for their valuable inputs and suggestions.

NAME AND SIGNATURE OF ALL THE ATTENDEES

Date: 04-07-2017

Sl.No.	Name	Signature
01	Aravinda K.	
02.	Dr. D. Seshachalam.	
03.	Dr. B.K. SUJATHA.	
04	PASUPULETI RAVISHANKER	
05	AVSS Ramya	
06	Dr. Preeta Sharan	
07	V. Dharmaraj	
08	DIVYA SHARMA	
09	Dr. NISHA KCR	
10	Lipsa Dash	

APPENDIX I

DIGITAL ELECTRONIC CIRCUITS			
Course Code	**: ECE33**	**Credits**	**:05**
L: P: T: S	**:3:2:0:0**	**CIE Marks**	**:50+25**
Exam Hours	**:03+03**	**SEE Marks**	**:50+25**

Course Outcomes: At the end of the Course, the student will have the ability to:

CO1	Recall the fundamental concepts of logic design
CO2	Demonstrate the simplification of Boolean expressions using standard methods
CO3	Utilize the knowledge of simplification by designing combinational logic circuits
CO4	Solve sequential logic circuits with the acquired knowledge of flip flops
CO5	Examine the significance of state machines in system design
CO6	Develop combinational and sequential circuits to meet the given specifications

Mapping of Course Outcomes to Program Outcomes:

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	-	-	-	-	3	-	-	3	-	-
CO2	3	3	3	3	-	-	-	-	3	3	-	3	-	-
CO3	3	3	3	3	-	-	-	-	3	3	-	3	-	-
CO4	3	3	3	3	-	-	-	-	3	3	-	3	-	-
CO5	3	3	3	3	-	-	-	-	3	3	-	3	-	-
CO6	3	3	3	3	1	-	-	1	3	3	-	3	-	-

Module No	Module Contents	Hrs.	COs
1	Principles of Combinational Logic: Binary Logic functions, Definition of combinational logic, Canonical forms, Generation of switching equations from truthtable, Karnaugh maps (3,4and5variables), Quine – McClusky Method, Map entered Variables.	9	CO1 CO2
	List of Experiments Simplification of Boolean expressions using K-map and realization of simplified expressions using basic and universal gates. Realization of Half/Full adder and Half/Full subtractor using logic gates.	4	
2	Analysis and design of combinational logic: General Approach to combinational logic, Decoders, Encoders, Digital Multiplexers, Adders and Subtractor- Cascading full adders, Look Ahead carry adder, Binary Comparators, Code Conversion	9	CO2 CO3
	List of Experiments (i)Realization of parallel adder/Subtractorsusing7483chip (ii) BCD to Excess-3 code conversion and vice versa. Realization of Binary to Gray code conversion and vice versa MUX/DEMUX – use of 74153, 74139 for arithmetic circuits and code Converter.	10	

	Realization of One/Two bit comparator and study of 7485 magnitude comparator. Use of a) Decoder chip to drive LED display and b) Priority encoder.		
3	Sequential Circuits – 1: Sequential circuit models, Basic Bi-stable Element, Latches-SR Latch, Application of SR Latch - A Switch Debouncer, $\overline{SR}$ Latch, The gated SR Latch, The gated D Latch, Timing Considerations, Flip-Flops- Latches, J-K Clocked Flip-Flops, Clocked T Flip-flop, Clocked D Flip-flop, The Master-Slave Flip-Flops, Edge Triggered Flip-Flop, catching 1s and 0s, Characteristic Equations	9	CO4
	List of Experiments Truth table verification of Flip-Flops: (i) JK Master slave(ii) T type and (iii) D type.	2	
4	Sequential Circuits – 2: Shift Registers: PIPO, SIPO, PISO, SISO, Universal Shift register. Counter: Ripple Counters, synchronous binary counter, Counters based on Shift Registers, Design of synchronous counters-Design of a Synchronous Mod-6 Counter using clocked JK Flip-Flops, clocked D, T, or SR Flip-Flops, Ring counter, Johnson counter	9	CO5 CO6
	List of Experiments Shift left; Shift right, SIPO, SISO, PISO, PIPO operations using 74S95. Realization of synchronous and asynchronous counters. (7476, 7490, 74192, 74193). 3. Realization of Johnson and Ring counter.	6	
5	Sequential Design: Moore and Mealy State models, state machine notations, Synchronous Sequential Circuit Analysis, Construction of state diagrams. Logic Families: RTL and DTL circuits, TTL (Open-Collector output)	9	CO4 CO6
	List of Experiments 1. Design and implementation of synchronous or clocked sequential circuits using Mealy and Moore model	2	

TEXT BOOKS:

1. Digital Logic: Applications and Design, JohnM.Yarbrough,CengageLearning,2015 reprint.
2. Digital Principles and Design,DonaldD.Givone,2003,TataMcGrawHillEdition2002.
3. Digital Logic and Computer Design: M. Morris Mano, Pearson Education

REFERENCE BOOKS**:**

1. Digital Fundamentals, Thomas Floyd, 11th edition, 2014, Pearson Education.
2. An Illustrative Approach to Logic Design, R.D.Sudhakar Samuel,2010,Pearson Education.

Assessment Pattern

CIE- Continuous Internal Evaluation

Theory (50 Marks)

Bloom's Taxonomy	Tests	Assignments	Quizzes	Co-Curricular Activities
Marks	**25**	**10**	**5**	**10**
Remember	5	-	-	-
Understand	5	5	-	-
Apply	10	5	5	5
Analyze	5	-	-	-
Evaluate	-	-	-	5
Create	-	-	-	-

Practical (25 Marks)

Bloom'sTaxonomy	Tests	Assignments	Quizzes
Marks	**20**	**-**	**5**
Remember	5	-	
Understand	10	-	5
Apply	5	-	
Analyze	-	-	
Evaluate	-	-	
Create	-	-	

SEE- Semester End Examination

Theory (50 Marks)

Bloom's Taxonomy	Tests
Remember	10
Understand	20
Apply	10
Analyze	10
Evaluate	-
Create	-

Practical (25 Marks)

Bloom's Taxonomy	Tests
Remember	5
Understand	10
Apply	10
Analyze	-
Evaluate	-
Create	-

ANALOG ELECTRONICS CIRCUITS			
Course Code	**:ECE34**	**Credits**	**:05**
L: P: T: S	**:3:2:0:0**	**CIE Marks**	**:50+25**
Exam Hours	**:03+03**	**SEE Marks**	**:50+25**

Course Outcomes: At the end of the Course, the student will have the ability to:

CO1	Apply the basic knowledge of BJT and FET devices for designing circuits
CO2	Analyze load line concepts for various BJT and FET biasing circuits
CO3	Determine the high frequency response for BJT and JFET amplifier circuits using AC Analysis
CO4	Compare the effect of feedback topologies in amplifier circuits
CO5	Illustrate the working principles of oscillators and power amplifiers
CO6	Model the applications of diode, BJT and FET circuits using discrete components and simulation tools

Mapping of Course Outcomes to Program Outcomes:

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO2
CO1	3	3	2	-	-	-	-	-	-	-	-	2	-	-
CO2	3	3	-	-	3	-	-	-	-	-	-	-	3	-
CO3	3	3	-	-	3	-	-	-	-	-	-	-	3	-
CO4	3	3	-	-	3	-	-	-	-	-	-	-	3	-
CO5	3	3	-	-	3	-	-	-	-	-	-	-	3	-
CO6	3	3	2	2	3	-	-	-	2	2	-	2	3	2

Module No	Module Contents	Hrs.	COs
1	BJT BIASING AND AC ANALYSIS: Transistor configurations (CE, CB,CC), Need for Biasing, Load Line and Q-point, Biasing Circuits- Fixed Bias, Emitter Bias ,Voltage Divider bias with their stability factors. Analysis of various bias configurations using re transistor model, Complete hybrid equivalent model. Numerical Examples.	9	CO1 CO2 CO6
	List of Experiments 1. Testing of Diode clipping (Single/Double ended) circuits. (Hardwired) 2. Testing of Clamping circuits: positive clamping /negative clamping. (Hardwired) 3.Testing of voltage multipliers: doublers, triplers, quadruplers.(Simulation using Multisim / Pspice)	6	

2	JFET BIASING AND AMPLIFIERS: Construction and characteristics of JFET, JFET configurations (CS,CG,CD), JFET Biasing (Fixed bias, Self bias and Voltage divider bias), JFET small signal model of various biasing. Numerical Examples.	9	CO1 CO2 CO6
	List of Experiments 1. Plotting the transfer curve of transistor switch (BJT, JFET,MOSFET). (Hardwired). 2. Wiring of RC coupled Single stage BJT amplifier and Determination of the gain-frequency response, input and output impedances. (Hardwired).	4	
3	BJT AND JFET FREQUENCY RESPONSE: Introduction (Logarithms and Decibels), Bode plots, Miller's theorem, Rise time-Bandwidth relationship, low and high frequency response of BJT stages and FET amplifiers.	9	CO3 CO6
	List of Experiments Wiring of RC coupled Single stage JFET amplifier and Determination of the gain-frequency response, input and output impedances. (Hardwired) Simulation of BJT Darlington Emitter follower with and without bootstrapping and determination of the gain, input and output impedances. (Simulation using Multisim / Pspice).	4	
4	FEEDBACK AND OSCILLATOR CIRCUITS: The feedback concept, Feedback connection types, Practical Feedback Circuits, Theory of Sinusoidal Oscillation, Phase Shift Oscillator, Wien Bridge Oscillator, Tuned Oscillator Circuits (Twin T, Colpitts, Hartley, Armstrong, Clapp), Crystal Oscillator, Uni-junction oscillator.	9	CO4 CO5 CO6
	List of Experiments Simulation of a two stage BJT Voltage series feedback amplifier and determination of the gain, Frequency response, input and output impedances with and without feedback. Wiring and Testing for the performance of BJT-RC Phase shift Oscillator for 10 KHz.(Hardwired) Testing for the performance of BJT–Hartley & Colpitts Oscillators for RF range. (Hardwired)	6	
5	POWER AMPLIFIERS: Introduction (Amplifier Types and Efficiency), Class A amplifier (Series fed, Transformer coupled), Class B amplifier (Transfer coupled push-pull, Complementary Symmetry), Amplifier Distortion, Power Transistor Heat Sinking, Class C and Class D amplifiers.	9	CO5 CO6
	List of Experiments Simulation of a transformer less Class–B push-pull power amplifier and determination of its conversion efficiency. Testing of Class-C tuned amplifier, measurement of conduction	4	

	angle and calculation of efficiency. (Hardwired)		

TEXT BOOKS:

1. Electronic Principles, Albert Malvino and David Bates, 7th edition, 2015, McGraw-Hill.
2. Electronic Devices and Circuit Theory, Robert L. Boylestad and Louis Nashelsky, 11th Edition, 2008, Pearson Education /PHI.

REFERENCE BOOKS:

1. Electronic Devices and Circuits, MillmanJ and Halkias C 3rd edition, 2007,TMH.
2. Equipment manuals as applicable.

Assessment Pattern

CIE- Continuous Internal Evaluation

Theory (50 Marks)

Bloom's Taxonomy	Tests	Assignments	Quizzes	Co-Curricular Activities
Marks	**25**	**10**	**5**	**10**
Remember	5	-	-	-
Understand	5	-	-	-
Apply	5	5	-	5
Analyze	10	-	5	-
Evaluate	-	5	-	5
Create	-	-	-	-

Practical (25 Marks)

Bloom'sTaxonomy	Tests	Assignments	Quizzes
Marks	**20**	-	**5**
Remember	10	-	-
Understand	5	-	5
Apply	5	-	-
Analyze	-	-	-
Evaluate	-	-	-

Create	-	-	-

SEE – Semester End Examination

Theory (50 Marks)

Bloom'sTaxonomy	Tests
Remember	20
Understand	10
Apply	10
Analyze	10
Evaluate	-
Create	-

Practical (25 Marks)

Bloom'sTaxonomy	Tests
Remember	10
Understand	5
Apply	10
Analyze	-
Evaluate	-
Create	-

LINEAR INTEGRATED CIRCUITS			
Course Code	**:ECE46**	**Credits**	**:03**
L: P: T: S	**:3:0:0:0**	**CIE Marks**	**:50**
Exam Hours	**:03**	**SEE Marks**	**:50**

Course Outcomes: At the end of the Course, the student will have the ability to:

CO1	Classify the basic building blocks and compare the various parameters of linear integrated circuits
CO2	Interpret the DC and AC characteristics of operational amplifiers, their effect on output, and the compensation techniques.
CO3	Apply the theory of op amps in applications of op amps related to analog signal processing domain/industry
CO4	Design various signal processing circuits and voltage regulators using linear and non linearICs.
CO5	Design of analog filters using operational amplifiers by utilizing an in depth understanding of its frequency response
CO6	Demonstrate the theory of ADC, DAC, TIMER and special purpose ICs.

Mapping of Course Outcomes to Program Outcomes:

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	-	-	-	-	-	3	3	-	-	3	-
CO2	3	3	3	3	-	-	-	-	3	3	-	-	3	-
CO3	3	3	3	3	-	-	-	-	-	-	1	3	3	3
CO4	3	3	3	3	3	1	-	-	3	-	-	3	3	3
CO5	3	3	3	3	3	-	-	-	-	-	-	-	3	3
CO6	3	3	3	3	3	-	-	-	3	3	-	3	-	3

Module No	Module Contents	Hrs.	COs
1	**OPERATIONAL AMPLIFIER FUNDUMENTALS:** Basic Op-Amp circuit, Op-Amp parameters – Input and output voltage, CMRR and PSRR, offset voltages and currents, Input and output impedances, Slew rate, Frequency limitations and effect of finite open loop gain. (Qualitative analysis). Op-Amps as DC Amplifiers-Direct coupled – Voltage Followers, Non-inverting Amplifiers, Inverting amplifiers, Summing amplifiers, Difference amplifier. Op-Amps as AC Amplifiers - Capacitor coupled Voltage Follower, Capacitor coupled Non-inverting Amplifiers, and Capacitor coupled Inverting amplifiers	9	CO1 CO2

2	**OP-AMP FREQUENCY RESPONSE AND COMPENSATION:** High input impedance - Capacitor coupled Voltage Follower, setting the uppercut- off frequency, Use of a single polarity power supply, Circuit stability, Frequency and phase response, Frequency compensating methods, Band width, Slew rate effects, Zin Mod compensation, and circuit stability precautions	9	CO2
3	**OP-AMP APPLICATIONS:** Voltage sources, current sources, Integrator and differentiator, Inverting and non-inverting summer, Log and antilog amplifiers, Instrumentation amplifier, Precision rectifiers, Limiting Circuits,Sampleandholdcircuits,Zerocrossingdetectors,InvertingSchmitt trigger circuits.	9	CO3 CO4
4	**FILTERS AND IC REGULATORS:** RC low-pass and high-pass circuit**,** Active Filters – First and second order Low pass & High pass filters, Band pass and Band Elimination filters, IC Voltage regulators, 723 general purpose regulator, Switching regulator.	9	CO4 CO5
5	**OTHER LINEAR IC APPLICATIONS:** 555 Timer and its differ circuit applications, High speed micro power timer (ALD1502), Precis waveform generator(ICL8038), PLL-operating principles, Ph detector/comparator, LM566VCO,D/A(R-2R) and A/D converters (S and counter type), Analog multipliers.	6	CO6

TEXT BOOKS:

1. Operational Amplifiers and Linear IC's, David A. Bell, 3rd edition,2011, Oxford University Press.
2. LinearIntegratedCircuits,D.RoyChoudharyandShailB.Jain,4th edition,2015, New Age International.
3. Pulse, Digital and Switching Waveforms, JacobMillmanandHerbertTaub,2000,TMH Edition.

REFERENCE BOOKS**:**

1. Opamps-Design,Applications and Troubleshooting, Terrell,3rd edition,2006, Elsevier.
2. OperationalAmplifiers,GeorgeClaytonandSteveWinder,5th edition,2008, Elsevier.
3. OperationalAmplifiersandLinearIntegratedCircuits,Robert.F.Coughlin&FredF. Driscoll, 2006,PHI/Pearson.
4. DesignwithOperationalAmplifiersandAnalogIntegratedCircuits,SergioFranco, 3rd edition, 2005,TMH.

Assessment Pattern

CIE- Continuous Internal Evaluation (50 Marks)

Bloom's Category	**Tests**	**Assignments**	**Quizzes**	**CO-Curricular Activities**
Marks (out of 50)	25	10	5	10
Remember	5	-	-	-
Understand	10	5	-	-
Apply	5	5	-	5
Analyze	5	-	5	-
Evaluate	-	-	-	5
Create	-	-	-	-

SEE- Semester End Examination (50 Marks)

Bloom's Category	**Tests**
Remember	15
Understand	15
Apply	10
Analyze	10
Evaluate	-
Create	-

MINI PROJECT-I			
Course Code	**:ECE37**	**Credits**	**:02**
L: P: T: S	**:0:2:0:0**	**CIE Marks**	**:25**
Exam Hours	**:03**	**SEE Marks**	**:25**

The student will have the ability to

	Course outcomes
CO1	Understand the methodologies of technical projects
CO2	Develop the product for the required specifications
CO3	Work as an individual or in a team in development of technical projects
CO4	Test the product for the required specification
CO5	Articulate the project related activities and findings
CO6	Enhance the idea of project for extended applications

Mapping of Course Outcomes to Program Outcomes:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	3	-	-	-	-	-	-	-	-	-	-
CO2	3	3	3	3	3	3	-	-	3	3	3	3	3	3
CO3	3	3	3	-	-	-	-	-	-	3	3	3	3	3
CO4	3	3	3	3	3	3	-	3	3	-	3	3	3	3
CO5	3	-	-	-	-	3	2	3	3	-	3	3	-	-
CO6	3	3	3	3	3	3	2	3	3	3	3	3	3	3

MINI PROJECT-II			
Course Code	**:ECE47**	**Credits**	**:02**
L: P: T: S	**:0:2:0:0**	**CIE Marks**	**:25**
Exam Hours	**:03**	**SEE Marks**	**:25**

The student will have the ability to

	Course outcomes
CO1	Identify the problem statement, objectives and methodologies to carry out the project
CO2	Analyze suitable hardware and software required to do the project
CO3	Design engineering solutions of the chosen project utilizing a comprehensive and systematic approach
CO4	Demonstrate technical aspects of application specific prototypes
CO5	Work as an individual or in a team work in development of technical projects
CO6	Articulate the project related activities and findings

Mapping of Course Outcomes to Program Outcomes:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	**3**	**-**	**-**	**-**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**3**
CO2	**3**	**3**	**-**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**3**
CO3	**3**	**3**	**3**	**3**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**3**
CO4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**-**	**3**	**3**	**3**	**3**
CO5	**3**	**3**	**3**	**-**	**-**	**-**	**-**	**3**	**3**	**3**	**3**	**3**	**-**	**-**
CO6	**3**	**-**	**-**	**-**	**-**	**3**	**3**	**3**	**3**	**-**	**3**	**3**	**-**	**-**

APPENDIX II

New Horizon College of Engineering, Bangalore

B.E. Program - Batch: 2016 -2020

Department of Electronics and Communication Engineering

Scheme of Third and Fourth Semester

Academic Year: 2017 – 2018

Second Year / Third Semester												
Sl. No.	**Course code**	**Course title**	**Credit Distribution**				**Overall credits**	**Theory hours**	**Lab hours**	**Marks**		
			L	**P**	**T**	**S**				**CIE**	**SEE**	**Total**
1	MAT31	Engineering Mathematics - III	4	0	1	0	5	6	0	50	50	100
	HSS322	Life Skills for Engineers	2	0	0	1	3	2	0	50	50	100
3	ECE33	Digital Electronic Circuits	3	2	0	0	5	3	4	75	75	150
4	ECE34	Analog Electronic Circuits	3	2	0	0	5	3	4	75	75	150
5	ECE35	Network Analysis	3	0	1	0	4	5	0	50	50	100
6	ECE36	Signals and Systems	3	0	0	0	3	4	0	50	50	100
7	ECE37	Mini project - 1	0	2	0	0	2	0	0	25	25	50
TOTAL							27	23	8	375	375	750
Second Year / Fourth Semester												
Sl. No.	**Course code**	**Course title**	**Credit Distribution**				**Overall credits**	**Theory hours**	**Lab hours**	**Marks**		
			L	**P**	**T**	**S**				**CIE**	**SEE**	**Total**
1	MAT41	Engineering Mathematics-IV	4	0	1	0	5	6	0	50	50	100
2	HSS421	Economics for Engineers	2	0	0	1	3	2	0	50	50	100

3	ECE43	System Design using HDL	3	2	0	0	5	3	4	75	75	150
4	ECE44	Digital Signal Processing	3	2	0	0	5	3	4	75	75	150
5	ECE45	Control Systems	3	0	1	0	4	5	0	50	50	100
6	ECE46	Linear Integrated Circuits	3	0	0	0	3	4	0	50	50	100
7	ECE47	Mini Project-II	0	2	0	0	2	0	0	25	25	50
TOTAL							27	23	8	375	375	750

New Horizon College of Engineering, Bangalore

B.E. Program - Batch: 2015 -2019

Department of Electronics and Communication Engineering

Scheme of Third and Fourth Semester

Academic Year: 2016 – 2017

Second Year / Third Semester												
Sl. No.	**Course code**	**Course title**	**Credit Distribution**				**Overall credits**	**Theory hours**	**Lab hours**	**Marks**		
			L	**P**	**T**	**S**				**CIE**	**SEE**	**Total**
1	16MAT31	Engineering Mathematics-III	4	0	1	0	5	6	0	50	50	100
2	16HSS322	Life Skills for Engineers	2	0	0	1	3	2	0	50	50	100
3	16ECE33	Programming with Data Structures	3	0	0	1	4	4	0	50	50	100
4	16ECE34	Electronic Circuits-I	4	1	0	0	5	4	3	75	75	150
5	16ECE35	Network Analysis	3	0	1	0	4	5	0	50	50	100
6	16ECE36	Signals and Systems	3	1	0	0	4	4	2	75	75	150
7	16ECE37	Logic Design	0	2	0	0	2	0	4	25	25	50
TOTAL							**27**	**25**	**9**	**375**	**375**	**750**

Second Year / Fourth Semester												
Sl. No.	**Course code**	**Course title**	**Credit Distribution**				**Overall credits**	**Theory hours**	**Lab hours**	**Marks**		
			L	**P**	**T**	**S**				**CIE**	**SEE**	**Total**
1	16MAT41	Engineering Mathematics-IV	4	0	1	0	5	6	0	50	50	100
2	16HSS421	Introduction to Economics	2	0	0	1	3	2	0	50	50	100
3	16ECE43	Electronic Circuits-II	4	1	0	0	5	4	3	75	75	150

4	16ECE44	Digital Signal Processing	4	1	0	0	5	4	3	75	75	150
5	16ECE45	Control Systems	3	0	1	0	4	5	0	50	50	100
6	16ECE46	System Design using HDL	4	1	0	0	5	4	3	75	75	150
TOTAL							**27**	**25**	**9**	**375**	**375**	**750**