

Department of Electronics and Communication Engineering

Academic Year 2020-2021

INDUSTRIAL TRAINING PROGRAM FOR FACULTY

On

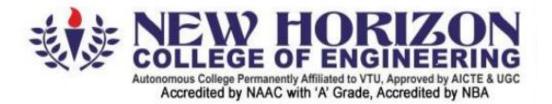
ASIC DESIGN FLOW USING MENTOR GRAPHICS

26.07.2021



I) INVITATION/POSTER OF THE EVENT





II) LIST OF PARTICIPANTS

S.No.	Name of the Participant	Designation
1.	Dr. Sanjeev Sharma	Professor & Head
2.	Dr. Mohan Kumar Naik B	Professor
3.	Dr. Aravinda K.	Associate Professor
4.	Dr. Jayanthi M.	Associate Professor
5.	Dr. Piruthiviraj.P	Associate Professor
6.	Dr. Rajesh.G	Associate Professor
7.	Dr. Gurulakshmi A. B	Associate Professor
8.	Dr.Santhosh Krishna B V	Assistant Professor
9.	Ms. Monika Gupta	Assistant Professor
10.	Ms. Nayana G. H.	Assistant Professor
11.	Mr. Ashok.K	Assistant Professor
12.	Ms.Aneeta S Antony	Assistant Professor
13.	Ms.Vansha Kher	Assistant Professor
14.	Ms. Ramanamma Parepalli	Assistant Professor
15.	Mr. Richard Lincoln Paulraj	Assistant Professor
16.	Mr.Puvirajan T	Assistant Professor



III) REPORT

Industrial Training Program for Faculty on ASIC Design Flow using Mentor Graphics in association with CoreEL Technologies was conducted on 26th July, 2021. The Session was delivered by **Mr. Ankur Sangal** Senior Application Engineer, CoreEL Technologies Bangalore and supported by **Bhanu Prakash Dixith B N** Associate Manager - University Relations CoreEL Technologies Bangalore. **Dr.P.Piruthiviraj**, Associate Professor /ECE is the faculty coordinator of the Program. During the session, the speaker has covered the Session on Full custom and Semi Custom Design. Faculties from Department of ECE have participated in this training program. Thereafter VLSI software demonstration is delivered as a Hands-on Session.

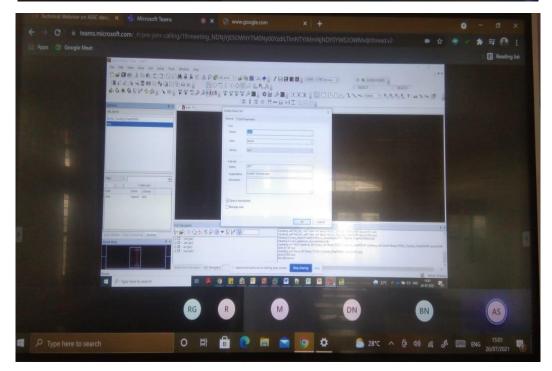
Outcome of the Industrial Training/FDP:

- EDA tool flow eliminates time consuming aspects of mixed signal development like polygon editing and layout verification.
- In view to provide a better exposure for the faculty and students in the Design and Verification of Digital Circuits using front-end and back-end tools the industrial training program has been designed.
- This training has given an invaluable resource for the participants, those who are trying to enhance their knowledge in the current needs of the VLSI Industry.



Accredited by NAAC with 'A' Grade, Accredited by NBA

Full-Custom IC Design Flow	
RegTracer copilure	Tape Out IC Fabrication
	Post-Layout /erification
Tanner S-edit	Physical /erification
Functional Verification (M	Layout fanual/SDL)



NEW HORIZON COLLEGE OF ENGINEERING DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING FEEDBACK FORM

INDUSTRIAL TRAINING PROGRAM FOR FACULTY

On

ASIC DESIGN FLOW USING MENTOR GRAPHICS

Instruction: Please put the rating in the appropriate column

Excellent-5, Good-4, Average-3, Satisfactory-2, Poor-1

S.No.	Participants	Instructor Knowledge on topic	Contents of the presentation	Guidance	Overall
1.	Dr. Sanjeev Sharma	4	5	5	4
2.	Dr. Mohan Kumar Naik B	4	4	4	4
3.	Dr. Aravinda K.	4	4	4	4
4.	Dr. Jayanthi M.	4	5	4	5
5.	Dr. Piruthiviraj.P	4	5	4	5
6.	Dr. Rajesh.G	4	5	4	5
7.	Dr. Gurulakshmi A. B	4	5	5	4
8.	Dr.Santhosh Krishna B V	4	5	5	4
9.	Ms. Monika Gupta	4	5	4	5
10.	Ms. Nayana G. H.	4	5	5	5
11.	Mr. Ashok.K	5	4	4	4
12.	Ms.Aneeta S Antony	5	4	5	4
13.	Ms.Vansha Kher	5	5	5	5
14.	Ms. Ramanamma Parepalli	5	4	5	5
15.	*	5	4	5	4
16.	Mr.Puvirajan T	4	4	4	4

Sougees

Signature of HOD