

## DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING <u>A REPORT ON SYSTEM VERILOG FOR VERIFICATIONWORKSHOP</u>

Workshop topic: Verification using System Verilog

Duration: 4 hours

N

Number of Student Attended: 52

This workshop was arranged for the global students of the ECE 2019-23 batch, under the guidance of the instructor Mr. Ravi Subramanian, from the institute 'Eklakshya Innovation Labs'. The duration of the workshop was for 4 hours on 21st November 2022.

The workshop was well structured with proper segregation of topic. They had organized a well-structured hands-on session for students where in the students were given access to their EDA platform and had hands-on session along with the instructor. Before the workshop commencement the students had received a mail to create our account in their assessment portal where we were given 4 pre-requisite assessment. The test was MCQ based and covered the topics of Verilog and HDL.

The instructor introduced the topic straight from the basics and was always available to clear the doubts of students. The workshop started off with teaching the theory first then moving on to the practical side of the topic. The tool used during the workshop was 'EDA Playground'. Started off with the basics of Verilog and slowly moving into the complex concepts of Verilog.

The session was an interactive one and covered all the topics planned for the workshop. We had to understand the concepts and along with the instructor worked on the EDA Playground tool as well. Few pictures of the workshop are also attached.

The workshop was successfully completed, which gave us an insight to how the basic verification procedures can be performed using a given FDA tool and how it can be extended onto the general application side of verification in real time. The trainer had been helpful throughout the entire duration of the workshop, which made us interested into the verification side of the VLSI industry.