New Horizon College of Engineering

Department of Electronics and Communication Engineering

BOARD OF STUDIES MEETING - 9

DATE: 26/11/2022

VENUE: Department of ECE (A 201)

Time: 10.00 AM to 11:00 AM

AGENDA

1. Syllabus of First Year Course BASIC ELECTRONICS (22ESC141/241)
2. Syllabus revision of 4th Semester Theory Course SYSTEM DESIGN USING HDL (21ECE45A)
3. Syllabus revision of 4th Semester Lab Course HARDWARE DESCRIPTION LANGUAGE LAB (21ECL45A)

25/11/2022.

MINUTES OF THE 9TH MEETING OF THE BOARD OF STUDIES DURING AY 2022-2023

1. Welcome and Introductory remarks by the BOS Chairman

The Chairman welcomed VTU Nominee, expert members from academics and industry and other members of the Board of Studies, and highlighted the following salient points for discussion in the 9th BOS Meeting:

- Approval for Syllabus of First Year Course "Basic Electronics"
- Approval for the syllabus revision of 4th Semester Theory Course "System Design Using HDL"
- Approval for the syllabus revision of 4th Semester Lab Course "Hardware Description Language Lab"

Introductory remarks by the BOS Chairman

i) Chairman remarked on the need of accreditation process which is predominantly outcome-based aiming at giving more weightage to the curriculum design, execution and outcome.

ii) Chairman mentioned about the recent guidelines proposed by VTU for the curriculum design of First year BE, and the number of courses to be offered for B.E. program under different baskets.

iii) Chairman narrated the proposed syllabus of "Basic Electronics" for the AY 2022-23, and presented the same to the committee members.

iv) Chairman outlined about the initiative of Industry Sponsored Lab, wherein Intel has come forward to technically sponsor the HDL Lab, so as to make the students globally competitive. The revised syllabus for the same was already shared with all of the external BoS members through Email.

v) Chairman sought opinion of industry experts on curriculum design and structure that could promote learning and impart industry-specific skills. He also invited responses from the external academic experts on the same.

Remarks by Academic Experts and Expert Members

i) Academic expert emphasized to include textbook related to Communication system and Embedded system for the title of the course "Basic Electronics". Also suggested to keep BJT followed by MOSFET in the Course Content.

ii) Expert Member suggested to include N-channel and P-Channel Enhancement MOSFET, Applications of BJT and MOSFET, Frequency response of BJT and Tank circuit, in "Basic Electronics" for the betterment of Students in Mini-project work.

iii) All Expert members appreciated the initiative of Industry sponsor HDL Lab.

2. The Board of Studies in Electronics and Communication Engineering recommended the following:

Revised syllabus for 4th semester HDL Theory & Lab and 1st year Basic Electronics syllabus to be forwarded for approval for the AY 2022-23.

3. Vote of Thanks by the Chairman - BOS

The meeting concluded with the vote of thanks by the chairman (HOD, ECE Department). He appreciated the comments from all the experts, faculty and student alumni for their valuable inputs and suggestions.

Syllabus of First Year Basic Electronics Course is enclosed with this MoM.

28.11.22

BoS-Chairman

Dr. [illegible]
Professor and HOD - ECE
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Dean-Academics

Dr R J Anandhi
Professor and Dean-Academics
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Ring Road, Bellandur Post
Bengaluru

Principal

BASIC ELECTRONICS

Course Code	: 22ESC141/241	Credits	: 03
L:T:P:S	: 3:0:0:0	CIE Marks	: 50
Exam Hours	: 03	SEE Marks	: 50

Course Outcomes: At the end of the Course, the Student will be able to:

CO1	Understand the operating principle of semiconductor devices and its applications.
CO2	Understand the concept of number systems.
CO3	Construct combinational and sequential circuits using the basic logic gates.
CO4	Discuss the principles and usage of Embedded systems.
CO5	Utilize the knowledge of modulation techniques in relating the generations of cellular communication systems.
CO6	Engage in independent learning as a member of a team, submit a report and use ICT for effective presentation of the study on assigned topics related to electronic systems.

Mapping of Course Outcomes to Program Outcomes:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-
CO3	3	3	-	-	-	-	-	-	-	-	-	-
CO4	3	3	-	-	-	-	-	-	-	-	-	-
CO5	3	3	-	-	-	-	-	-	-	-	-	-
CO6	2	2	2	2	2	-	-	-	2	2	-	2

SYLLABUS

Sl no	Contents of Module	Hrs	COs
1	**Semiconductor Diodes and Applications:** P-N Junction diode – its principle, characteristics and parameters Applications: Half-Wave Rectifier, Full Wave Rectifier (Two Diode, Bridge Rectifier), Zener diode as Voltage regulator. Textbook 1: 1.6, 1.7, 2.2, 3.1, 3.2, 9.5 **Bipolar Junction Transistor:** BJT Operation, BJT Voltages and Currents, BJT as a switch, Common Emitter Characteristics, Numerical examples as applicable. Textbook 1: 4.1, 4.2, 4.4, 4.6	8	CO1,CO6

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2	**MOSFET:** Introduction to MOSFET theory, Operation and characteristics of Enhancement MOSFET for n-channel, MOSFET as a switch. Comparison between BJT and MOSFET. Textbook 1: 9.5 **BJT as an Amplifier:** Biasing - DC load line, Need for biasing, Single stage CE amplifier using Voltage divider bias. Textbook 1: 5.1, 5.4, 6.4 (excluding h-parameter analysis) **Oscillator:** Barkhausen criterion, Conceptual discussion of Crystal controlled oscillator. Textbook 1: 16.1, 16.9	8	CO1,CO6
3	**Number Systems:** Introduction, Number Systems (Decimal, Binary, Hexadecimal, Octal), Conversion from one number system to other, Complement of Binary Numbers (1's and 2's), Binary subtraction using 1's and 2's complement. **Digital Electronics:** Logic gates, NAND and NOR as universal gates, Boolean Algebra Theorems, De Morgan's theorem, Algebraic Simplification. Textbook 2: 1.2, 1.3, 1.4, 1.5, 2.1, 2.2, 2.3, 2.4, 2.7	8	CO2,CO3,CO6
4	**Building blocks of a Digital system:** Combinational circuits (Half Adder, Full Adder), Sequential circuits (SR Latch using NAND gates, Flip-Flops [SR, JK, D, T]). Textbook 2: 4.3, 5.5, 6.2, 7.2 **Embedded Systems:** Definition of an Embedded System, Embedded systems vs General Purpose Systems, Application of Embedded Systems, Purpose of Embedded systems, Characteristics of Embedded systems. Reference book 1: 1.1, 1.2, 1.5, 1.6, 3.1	8	CO3,CO4,CO6
5	**Communication Systems:** Introduction to communication systems, Need for modulation, Principles of amplitude modulation, Introduction to angle modulation, FM and PM waveforms, Amplitude shift keying, Frequency shift keying, Phase shift keying. Textbook 3: 1.3, 1.4, 4.1, 4.2, 7.5, 9.3, 9.4, 9.5 1G, 2G cellular telephone systems – GSM, 3G and 4G, Simplified block diagram of a digital radio system. Textbook 3: 19.3, 20.2, 20.4, 20.9.2, 9.1	8	CO5,CO6

Text Books:

1. Electronic Devices and Circuits, David. A. Bell, 5th edition, 2008, Oxford University Press.
2. Digital Logic and Computer Design, M. Morris Mano, 5th edition, 2002, PHI.
3. Electronic communication systems, Wayne Tomasi, 5th edition, 2001, Pearson education.

Reference Books & Website:

1. Introduction to Embedded systems, Shibu K.V., 1st Edition, McGraw Hill Education, 2009.
2. Principles of Electronics, V. K. Mehta, 12th edition, 2020, S. Chand Publishing.
3. https://www.rfpage.com/evolution-of-wireless-technologies-1g-to-5g-in-mobile-communication/

Assessment Pattern

CIE- Continuous Internal Evaluation (50 Marks)

Bloom's Category	Tests	Assignment	Quiz	Mini Project
Marks (out of 50)	25	5	10	10
Remember	10	-	5	-
Understand	10	-	5	-
Apply	5	5	-	-
Analyze	-	-	-	10
Evaluate	-	-	-	-
Create	-	-	-	-

SEE- Semester End Examination (50 Marks)

Bloom's Category	Tests
Remember	10
Understand	20
Apply	15
Analyze	5
Evaluate	-
Create	-

NEW HORIZON COLLEGE OF ENGINEERING

AUTONOMOUS COLLEGE Permanently Affiliated to VTU, Approved by AICTE & UGC
Accredited by NAAC with 'A' Grade

Department of Electronics and Communication Engineering

Board of Studies (BOS) meeting

26th November 2022 at 10.00am

List of BoS members present:

S.No	Name of the staff	Signature
1	Dr. SIDDESH G.K.	Siddesh
2.	Dr. Sanjeev Sharma	
3	Prof. Binod Kumar Sinha	
4	Dr Pinthiviraj P	
5	Dr. M. Dhivya	26/11/22
6	Arun Kumar	
7.	Dr Rajesh G	26/11/22
8.	Dr. A.B. Gunduvalakshmi	A.B. Gunduvalakshmi 26/11/22
9.	P. Ranganna	
10.	Dr. Aravinda K.	
11.	Dr. Ravi, GAT	Joined online
12.	Dr. Bhargavi, SJCIT	
13.	Dr. Shivananda, CIT	
14.	Mr. Aksharamurali	

Aravinda K
26.11.22

16.11.2022

To

The Principal,
New Horizon College of Engineering,
Bengaluru – 560 103.

Through

The Dean (Academics),
New Horizon College of Engineering,
Bengaluru – 560 103.

Sub: Syllabus upgradation for the course SYSTEM DESIGN USING HDL (21ECE45A)

Respected Sir,

We are happy to inform you that INTEL has come forward to sponsor our HDL lab, and also to freely offer INTEL FPGA kits for the practice of our students. In this regard, Mr. Padmanaban K. (Software Enabling and Optimization Engineer, Intel) had suggested some changes in our Lab syllabus as well as some minor changes in our Theory syllabus. We have incorporated those changes which are feasible for our syllabus coverage, and have kept 4 experiments in the lab syllabus as Open-Ended ones.

As these changes are in line with the demand of the industry and the latest trends in future technology, we request you to kindly approve the syllabus modification and permit to incorporate the same in the upcoming semester (NEP Scheme - 4th semester).

Thanking You,

Aravinda K.

(HoD-ECE)

Encl: The revised syllabus for 21ECE45A and 21ECL47A

To HOD/ECE & BOS Chairman (ECE)

Respected Sir,

kindly send a copy of the revised syllabus from external BOS members too, for his views.

Approved. 22/11/22.

22/11/2022

NEW HORIZON COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

UPGRADATION OF SYLLABUS FOR

SYSTEM DESIGN USING HDL (21ECE45A) AND

HARDWARE DESCRIPTION LANGUAGE LAB (21ECL45A)

In line with the demand of the industry and the latest trends in future technology, a few changes are incorporated in the Theory syllabus of SYSTEM DESIGN USING HDL (21ECE45A) and in the HARDWARE DESCRIPTION LANGUAGE LAB (21ECL45A). The changes when compared with the earlier syllabus are as follows:

In Theory: SYSTEM DESIGN USING HDL (21ECE45A)

Module No.	Topics excluded	Topics included
5	• Design flow of FPGAs • Implementing Functions in FPGAs • Design Translation (synthesis) • Mapping • Placement and Routing	• Organization of FPGAs(Intel) • Programming file generation • Implementation on Intel FPGA boards

In Lab: HARDWARE DESCRIPTION LANGUAGE LAB (21ECL45A)

Experiments excluded	Experiments included
• Synthesize the code of above experiments and generate gate level netlist. • Encoder (without priority and with priority • Multiplexer and De multiplexer • Write an HDL code to realize all logic gates.	• Quartus Prime Design Software tool flow • Timers and Real-Time Clocks • Finite State Machines • Memory Blocks • A Simple Processor • An Enhanced Processor • Implement Algorithms in Hardware • Basic Digital Signal Processing

Note: In the Experiments included, the last 4 experiments are kept under Open Ended ones.

Included Reference Website:

https://www.intel.com/content/www/us/en/developer/topic-technology/fpga-academic/materials-digital-logic.html

In this syllabus modification, the following members were present and have reviewed the syllabus:

Module Coordinator	Ms. Nayana G H	Nayana G H
Course Coordinator	Mr. Richard Lincoln Paulraj	Richard Lincoln Paulraj
BOS Members	Dr. Sanjeev Sharma	
	Dr. Siddesh G. K.	Siddesh
	Dr. Jayanthi M.	Mjayanthi
	Dr. Piruthiviraj P.	P Piruthiviraj
	Dr. Gurulakshmi A. B.	A B. Gurulakshmi
	Dr. Dhivya M.	
	Dr. Rajesh G.	G. Rajesh
	Ms. Ramanamma	

BoS Chairman

Dean (Academics)

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Principal

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System Design using HDL

Course Code : 21ECE45A | Credits : 03

L:T:P: 2:1:0 | CIE Marks : 50

Exam Hours : 03 | SEE Marks : 50

Course Outcomes: On completion of the course, students should be able to:

21ECE45A.1	Recognize the importance of HDL for the automation of VLSI design
21ECE45A.2	Employ VHDL and / or Verilog data types and operators for describing the electronic hardware
21ECE45A.3	Examine the usage of various types of assignments in Verilog
21ECE45A.4	Identify the need of synthesis in the implementation of HDL
21ECE45A.5	Write Verilog code for the design of specific applications
21ECE45A.6	Distinguish between the commonly used programmable devices

Mapping of Course Outcomes to Program Outcomes:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
19ECE43	System Design using HDL													
19ECE43.1	3	3	-	-	-	-	-	-	-	-	-	-	1	1
19ECE43.2	3	3	3	-	-	-	-	-	-	-	-	-	1	1
19ECE43.3	3	3	3	-	-	-	-	-	-	-	-	-	1	1
19ECE43.4	3	3	3	2	-	-	-	-	-	-	-	-	2	2
19ECE43.5	3	3	2	2	-	-	-	-	-	-	-	-	2	2
19ECE43.6	3	3	2	2	-	1	-	-	-	-	1	-	2	2

Correlation levels: 1-Slight(Low) 2-Moderate(Medium) 3-Substantial(High)

10.11.22

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Module No	Module Contents	Hours	COs	RBT levels
1	**INTRODUCTION TO VHDL:**A brief history of HDL, Structure of HDL module, Design Flow, Translation of VHDL Code into a Circuit, Operators, Data types, Types of Descriptions(Behavioral, structural, Data-flow), Procedures and functions, Brief comparison of VHDL and Verilog. **(Text 1 - chapter 1,6; Text 3 - chapter 1)**	09	CO1, CO2, CO3	L1,L2, L3
2	**INTRODUCTION TO VERILOG:** Computer-Aided Design, Hardware Description Languages, Verilog Data Types and Operators, Verilog Description of Combinational Circuits, Verilog Modules, Verilog Assignments**(Text 2 – chapter 2)**	09	CO1, CO2, CO3	L1,L2, L3
3	Procedural Assignments, Modeling Flip-Flops Using Always Block, Always Blocks Using Event Control Statements, Verilog Models for Multiplexers, Modeling Registers and Counters Using Verilog Always Statements, Behavioral and Structural Verilog. SRAM model , **(Text 2 – chapter 2, 8.6)**	09	CO1, CO2, CO3	L1,L2, L3,L4
4	**SIMULATION AND SYNTHESIS:** Delays in Verilog, Compilation, Simulation, and Synthesis of Verilog Code, Simple Synthesis Examples. Constants, Arrays, Loops in Verilog, Testing Verilog Model, Verilog functions, Verilog Tasks, System functions **(Text 2 – chapter 2,8)** **DESIGN EXAMPLES:** A BCD Adder. 32-Bit Adders, Array Multiplier. **(Text 2 – chapter 4)**	09	CO3, CO5	L2, L3
5	**INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES AND DESIGNING WITH FPGA:** Brief Overview of Programmable Logic Devices. Simple Programmable Logic Devices (SPLDs)- Read Only Memories, Programmable Logic Arrays, Programmable array Logic. Complex Programmable Logic Devices (CPLDs). Field Programmable Gate Arrays (FPGAs) - Organization of FPGAs(Intel), FPGA Programming techniques, Programmable Logic block Architecture, Programming file generation, Implementation on Intel FPGA boards **(Text 2 – chapter 3,6 & Reference Website)**	09	CO4,C06	L2, L3

TEXT BOOKS:

1. HDLProgramming(VHDLandVerilog),NazeihM Botros,2015,John-WeilyIndiaPvt.Ltd
2. DigitalSystemdesignUsingVerilog,CharlesH RothJr.,LizyKurianJohn,ByeongKilLee, 1st Edition, 2015, CLEngineering.
3. Volnei A. Pedroni, "Circuit Design with VHDL", The MIT Press, 2004.

REFERENCE BOOKS:

1. Digital Systems Design using VHDL, Charles H Roth,Jr., 2007, Thomson
2. DigitalDesign:AnEmbeddedSystemsapproachUsingVERILOG,PeterJ.Ashenden,2014, Elesvier
3. J Bhaskar, "A Verilog HDL Primer (3/e)", Kluwer, 2005.

REFERENCE WEBSITE:

www.intel.com

Mapping of CO v/s PSO:

COs	PSO 1	PSO 2
19ECE43	System Design Using HDL	
CO1	1	1
CO2	1	1
CO3	1	1
CO4	2	2
CO5	2	2
CO6	2	2

Assessment Pattern

CIE- Continuous Internal Evaluation Theory (50 marks)

Bloom's Taxonomy	Tests	Assignments	Quizzes
Marks	25	15	10
Remember	5	-	5
Understand	5	-	5
Apply	10	5	-
Analyze	5	5	-
Evaluate	-	5	-
Create	-	-	-

SEE- Semester End Examination Theory (50 Marks)

Bloom's Taxonomy	Tests
Remember	10
Understand	20
Apply	20
Analyze	-
Evaluate	-
Create	-

Hardware Description Language Lab	
Course Code: 21ECL45A	Credits: 1
L: T: P: S 0:0:1:0	CIE Marks: 50
Exam Hours: 3	SEE Marks: 50

Course outcomes: On the completion of this laboratory course, students will be able to:

CO1	Write the Verilog /VHDL programs to simulate Combinational circuits in Dataflow, Behavioral and Gate level Abstractions.
CO2	Describe sequential circuits like flip flops and counters in Behavioral description and obtain simulation waveforms.
CO3	Design and verify the functionality of digital circuit/system by writing test benches
CO4	Program FPGAs to synthesize the digital designs.

Mapping of Course Outcomes to Program Outcomes:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
21ECL45A	21ECL45A - HARDWARE DESCRIPTION LANGUAGE LAB													
CO1	3	3	3	3	1	1	-	-	2	2	1	2	3	2
CO2	3	3	3	3	1	1	-	-	2	2	1	2	3	2
CO3	3	3	3	3	1	1	-	-	2	2	1	2	3	2
CO4	3	3	3	3	2	1	1	1	2	2	1	2	3	2

Correlation levels: 1-Slight(Low) 2-Moderate(Medium) 3-Substantial(High)

Sl.no	Laboratory Experiments	COs	RBT levels
1	Quartus Prime Design Software tool flow (www.intel.com) Write an HDL code to describe the functions of a Full Adder using three modeling styles. **(Text1 – chapter 1, Text2- chapter2)**	CO1,CO2,CO3,CO4 CO1,CO3	L1, L2, L3

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2	Write a model for 16 bit ALU using the 4bit opcodes; the requisite functions can be defined for the chosen opcodes. **(Text1 – chapter 1, Text2- chapter2)**	**CO1,CO3**	**L1, L2, L3**
3	a) Write an HDL program for the following designs: **a.** Decoder & Encoder **(Text1 – chapter 1, Text2- chapter2)** b) Develop the HDL code for the following flipflops: T, D, SR, JK. **(Text1 – chapter 1, Text2- chapter 2)**	**CO1,CO3** **CO2,CO3**	**L1, L2, L3**
4	Write an HDL program for the following designs: a. 4 bit Binary to Gray converter b. 4-bit Binary Comparator **(Text1 – chapter 1, Text2- chapter 2)**	**CO1,CO3**	**L1, L2, L3**
5	Design 4bit Binary and BCD counters (Synchronous reset and Asynchronous reset and "any sequence" counters). **(Text1 – chapter 1, Text2- chapter 2)**	**CO2,CO3**	**L1, L2, L3**
6	Synthesize the code of above experiments and generate gate level netlist. **(Text2- chapter 2)**	**CO4**	**L1, L2, L3**
7	Study the use of clocks in timed circuits: Timers and Real-Time Clocks **(Reference Website)**	**CO3,CO4**	**L2, L3,L4**
8	Implement a finite state machine (FSM) that recognizes two specific sequences of applied input symbols, namely four consecutive 1s or four consecutive 0s. **(Reference Website)**	**CO2,CO3**	**L2, L3,L4**
9	Examine the general issues involved in implementing Memory Blocks **(Reference Website)**	**CO2,CO3**	**L2, L3,L4**
10	Write an HDL code to display messages on the given seven segment display **(Text2- chapter 2,3,6)**	**CO3,CO4**	L2, L3, L4
11	Write the HDL code to control speed, direction of dc and stepper motor **(Text2- chapter 2,3,6)**	**CO3,CO4**	**L2,L3,L4**
12	Write the HDL code to generate different waveforms (sawtooth, sine wave, square, triangle, ramp etc) using DAC and FPGA kit **(Text2- chapter 2,3,6)**	**CO4**	**L2, L3,L4**
	OPEN ENDED EXPERIMENTS		
13	Design and implement a simple processor. **(Reference Website)**	**CO1,CO2,CO3,CO4**	**L2, L3,L4**
14	Extend the capability of the processor: An Enhanced Processor. **(Reference Website)**	**CO1,CO2,CO3,CO4**	**L2, L3,L4**

15	Using algorithmic state machine charts, implement algorithms as hardware circuits. **(Reference Website)**	**CO1,CO2,CO3,CO4**	**L2, L3,L4**
16	Implement Basic Digital Signal Processing using the audio coder/decoder (CODEC) on the DE1-SoC or DE2-115 board. **(Reference Website)**	**CO1,CO2,CO3,CO4**	**L2, L3,L4**

TEXT BOOKS:

1. HDL Programming (VHDLandVerilog),Nazeih M.Botros, 2015, John-Weily India Pvt.Ltd
2. Digital System design Using Verilog, Charles H.RothJr., Lizy Kurian John, Byeong Kil Lee, 1st Edition, 2015, CL Engineering.
3. Volnei A. Pedroni, "Circuit Design with VHDL", The MIT Press, 2004.

REFERENCE BOOKS:

1. Digital Systems Design using VHDL, Charles H Roth,Jr., 2007, Thomson
2. Digtal Design:An Embedded Systems approach Using VERILOG, Peter J. Ashenden, 2014, Elesvier.
3. Verilog HDL: A Guide to Digital Design and Synthesis, Second Edition , Samir Palnitkar, Prentice Hall, 2003

REFERENCE WEBSITE:

https://www.intel.com/content/www/us/en/developer/topic-technology/fpga-academic/materials-digital-logic.html

Mapping of CO v/s PSO:

CO	PSO1	PSO2
21ECL45A	System Design using HDL Lab	

CO1	3	2
CO2	3	2
CO3	3	2
CO4	3	2

Assessment Pattern

CIE- Continuous Internal Evaluation (50 Marks)

Bloom's Taxonomy	Test	Conduction	Viva	Observation	Record
Marks	**25**	**10**	**5**	**5**	**5**
Remember	5	-	-	-	5
Understand	5	5	-	-	-
Apply	10	5	-	5	-
Analyze	5	-	5	-	-
Evaluate	-	-	-	-	-
Create	-	-	-	-	-

SEE- Semester End Examination(50 Marks)

Bloom's Taxonomy	Tests	Write-up	Conduction	Viva
Marks	**50**	**10**	**30**	**10**
Remember	10	-	15	-
Understand	10	5	-	-
Apply	20	5	15	-
Analyze	10	-	-	10
Evaluate	-	-	-	-
Create	-	-	-	-

New Horizon College of Engineering

(Autonomous College affiliated to VTU, Accredited by NAAC with 'A' grade)

Department of Electronics and Communication Engineering

External Board of studies (BOS) member Review on

Latest Syllabus of "Basic Electronics" and Revised Syllabus of "HDL Lab"

Date: 25-11-2022

The following topics could be included:

Module-1

1. Applications of MOSFET.
2. MOSFET as a switch.

Module-2

1. Transistor configurations.
2. BJT as a switch.
3. Frequency response of an amplifier and bandwidth concepts.
4. Types of Oscillators, tank circuit elements.

Module-3

1. Why NAND and NOR gates are called as Universal gates?
2. Boolean expression realizations using basic gates and universal gates.

Module-4

1. MUX and DEMUX.
2. Basics on microprocessor and microcontrollers.

Module-5

1. Basic block diagram of a communication system.
2. What is modulation? Need of modulation.
3. Concepts on analog modulation and digital modulations.

Name: Dr. SHIVANANDA

Designation: Associate Professor

Affiliation/ Organisation: Cambridge Institute of Technology,
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