Title	Alumni Talk on "**VLSI-IC Design Flow and Timing Analysis**"	
Department	Electronics and Communication Engineering	
Date	From :8th January 2024	To : 8th January 2024
Time	From : 10 AM	To: 11 AM
Brief Description (4-5 Lines Max)	Department of Electronics and Communication Engineering conducted an International alumni talk on "**VLSI-IC Design Flow and Timing Analysis**" on 8th January 2024(Venue: Falconry Seminar Hall).The speaker, **Naveen K H**, is an alumnus of ECE department (Batch-2015-2019). He is currently working as Physical Design Engineer with Soctronics Pvt Ltd. Naveen is having an overall experience of 5+ years in physical design. He is having good knowledge about ASIC Design Flow, Floor Planning, Power Planning, Placement, CTS, Routing and STA stages. The speaker spoke about the IC design flow and timing analysis. He also discussed about the skill sets required for the placement in VLSI industries. Students interacted with the speaker at the end of the session by taking suggestions and clarifying doubts on placement opportunities in core domain. The session was overall very informative.