NEW HORIZON
COLLEGE OF ENGINEERING
New Horizon Knowledge Park, Ring Road, Marathalli
Autonomous College Permanently Affiliated to VTU, Approved by AICTE & UGC
Accredited by NAAC with 'A' Grade, Accredited by NBA

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

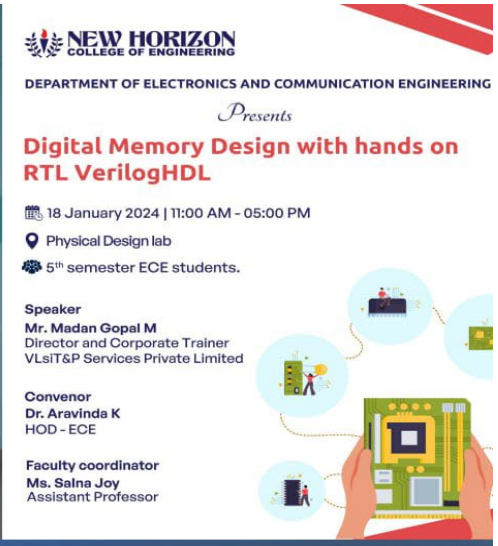
DIGITAL MEMORY DESIGN WITH HANDS-ON RTL VERILOG HDL

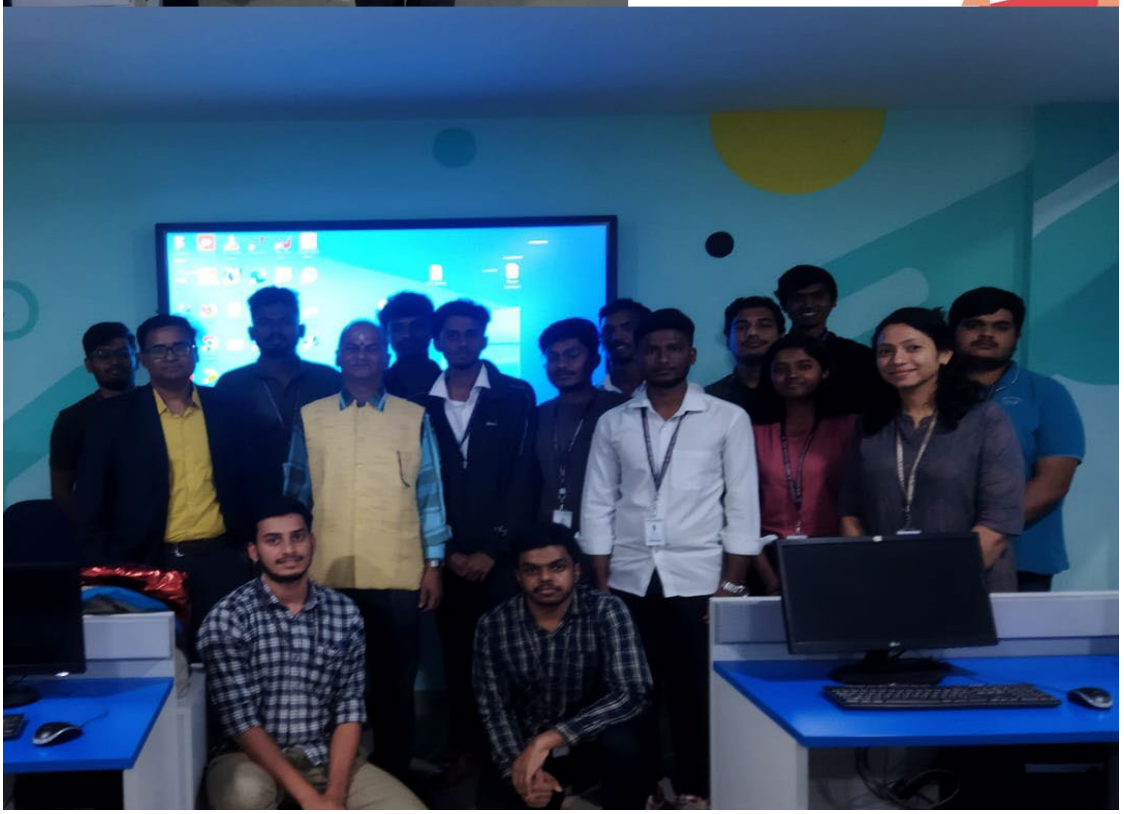
Date	:18-01-2024
Duration	:11 am-5 pm
Workshop topic	: Digital Memory Design with Hands-on RTL Verilog HDL
Number of Participants	:24
Resource person	:Mr Madan Gopal. M (Persuing Ph.D VLSI HLS FPGA), Director and Corporate Trainer, VLSIT&P Services Private Limited. www.vlsitnp.co.in

On January 18th, 2024, a comprehensive workshop on "Digital Memory Design with Hands-on RTL Verilog HDL" was conducted in the VLSI Lab. The workshop was aimed at 5th-semester students, providing them with a deep dive into digital memory design and practical experience with RTL Verilog HDL. Mr. Madan Gopal. M, pursuing a Ph.D. in VLSI HLS FPGA and serving as the Director and Corporate Trainer at VLSIT&P Services Private Limited, was the resource person for the workshop. His expertise and industry experience enriched the sessions, providing valuable insights to the participants

The workshop covered a range of topics essential for understanding digital systems. Participants were introduced to fundamental concepts laying the groundwork for the subsequent sessions.A detailed explanation of the rules governing port connections in digital systems was provided. Practical sessions allowed participants to implement gate level models, reinforcing theoretical knowledge. Participants engaged in hands-on activities to understand and implement dataflow modeling. This session focused on behavioral modeling, providing practical examples to enhance participants' skills. Mr. Madan Gopal shared insights into effective debugging techniques, an essential skill in digital system design. Real-world examples of Register-Transfer Level (RTL) designs were discussed, providing participants with practical exposure. Finite State Machine (FSM) design principles were covered with practical examples, aiding in the understanding of sequential logic. The workshop concluded with a detailed session on RTL memory modeling, a crucial aspect of digital memory design.

The workshop proved to be highly beneficial for the 24 participants, offering a comprehensive understanding of digital memory design and hands-on experience with RTL Verilog HDL. The practical approach and real-world examples shared by Mr. Madan Gopal enhanced the participants' skills in digital system design. The event was a success in aligning academic knowledge with practical applications in the field of VLSI and digital design. The participants expressed satisfaction with the hands-on approach, which enhanced their practical skills in digital system design. Overall, the workshop was a valuable contribution to the participants' academic and professional growth in the field of VLSI design.





FACULTY COORDINATOR HOD

Participants list

No	Name	USN	Section	Signature	
				9.30am-12.30pm	1.30pm-4pm
1	Athul Satheesh	1NH21EC025	A		
2	Brunda V	1NH21EC032	A		
3	Chiranthana M Reddy	1NH21EC038	A		
4	Gnanesh H Nayak	1NH21EC059	A		
5	Dikshitha NR	1NH21EC047	A		
6	Chirag V	1NH21EC037	A		
7	Santhosh	1nh22ec411	A		
8	B ROHAN SRIVATSAV	1NH21EC026	A		
9	Deepak H	1NH22EC403	A		
10	Dhimanth M	1NH21EC045	A		
11	A LEELA SAGAR	1NH21EC001	A	Ab	
12	Diwakar V	1NH21EC049	A		
13	Likhith kumar N	1NH22EC405	A		
14	Akhil Naik G	1NH21EC011	A	Ab	
15	Mohaka.R	1NH21EC094	B	Ab	
16	Om Prakash A	1NH21EC114	B		
17	Mithun S	1NH21EC093	B		
18	Gunturu Chiranjeevi	1NH21EC062	B	Ab	
19	H S Yashas	1NH21EC063	B		
20	Naresh Kumar R	1NH21EC106	B		
21	Sachin L	1NH22EC410	B		
22	Adithya N	1NH22EC400	B		
23	M Chandana	1NH21EC084	B		
24	Kriti Sujai Kumar Devatha	1NH21EC079	B		
25	Swarup m	1NH21EC085	B	Ab	
26	Mahi Prajwal Pagolu	1NH21EC087	B	Ab	
27	Kiran kumar p	1NH21EC117	B		
28	Mahalakshmi Y M	1NH22EC406	B	Ab	
29	Yashasvi Linga Reddy	1NH21EC190	C	Ab	
30	PRUTHVIRAJ K G	1NH21EC122	C		
31	shankarappa y	1NH21EC144	C		
32	SYED HANNAN	1NH21EC159	C	Ab	
33	Shashank C R	1NH21EC146	C		
34	S V harshitha	1NH21EC133	C	Ab	