

Title	VLSI-IC Design Flow and Timing Analysis	
Department	Electronics and Communication Engineering	
Date	From :15 Th October 2024	To : 15 th Ovtober 2024
Time	From : 10 AM	To: 11 AM
Brief Description (4-5 Lines Max)	<p>Department of Electronics and Communication Engineering conducted an International alumni talk on “IC Design Flow and Core VLSI Career Opportunities” on 15th October 2024(Venue: Tejas Seminar Hall).The speaker, Naveen K H, is an alumnus of ECE department (Batch-2015-2019). He is currently working as Physical Design Engineer with Qualcomm. Mr Naveen has overall experience of 5+ years in physical design. Mr Naveen’s expertise include ASIC Design Flow, Floor Planning, Power Planning, Placement, CTS, Routing and STA stages.</p> <p>The speaker briefed the participants about the IC design flow and timing analysis. He also discussed about the skill sets required for the placement in VLSI domain. Students interacted with the speaker at the end of the session. The session was overall very informative</p>	



NEW HORIZON
COLLEGE OF ENGINEERING
New Horizon Knowledge Park, Ring Road, Marathalli
Autonomous College Permanently Affiliated to VTU, Approved by AICTE & UGC
Accredited by NAAC with 'A' Grade, Accredited by NBA



Alumni Talk

Alumni Association
and
Department of Electronics and Communication Engineering

**IC Design Flow and Core
VLSI Career Opportunities**

